MXV11-B MULTIFUNCTION OPTION MODULE

GENERAL

The MXV11-B is a multifunction option module used with the PDP-11/23 and KDJ11 processor systems. The MXV11-B read/write memory contains 128K bytes of dynamic MOS RAM without parity. The MXV11-B is configured from 64K SIPS (single inline package). Four SIPS provide 128K bytes (64K words) of memory storage. Battery backup is supplied when jumpers are configured to enable that feature and system supplied power is connected. This dual-height, multifunction module option can operate on a 22-bit Q-Bus system, (up to 316 words) on an 18- and 16-bit Q-Bus system unit.

Features

W/R MOS RAM memory
5 V battery backup for MOS RAMs
Read only memory (ROM)
ROM window map logic (page control register)
Two asynchronous, serial line ports (SLU0 and SLU1)
Multiple LTC frequencies
LED diagnostic display register

Electrical Specifications

Power Requirements – The following voltages are used by this module.

Voltage	Tolerance	Pins
+5 V	±5%	AA2 BA2, BV1
+12 V	±5%	AD2, BD2
+5 VB	±5%	AV1

Power dissipated in each power supply configuration is as follows.

No battery backup

+5 V		+12 V	
Typ	17.25 W	Typ	0.67 W
Max	24.57 W	Max	0.71 W

Battery backup configuration

+5 V		+5 VB		+12 V	
Typ	12.90 W	Typ	4.35 W	Typ	0.67 W
Max	15.95 W	Max	8.60 W	Max	0.71 W

Data retention mode

VCC = 0 V, +12 V supply = 0

+5 VB

Typ	4.35 W
Max	5.54 W

Related Documentation

MXV11-B Technical Manual (EK-MXV1B-TM)
MXV11-B User Guide (EK-MXV1B-UG)
MXV11-B2 ROM Set User Guide (EK-MXVB2-UG)
MXV11-B Multifunction Option Module User Guide (EK-MXV1B-UG)
MXV11-B Field Maintenance Print Set (MP-01469-00)

Program Options and Defaults

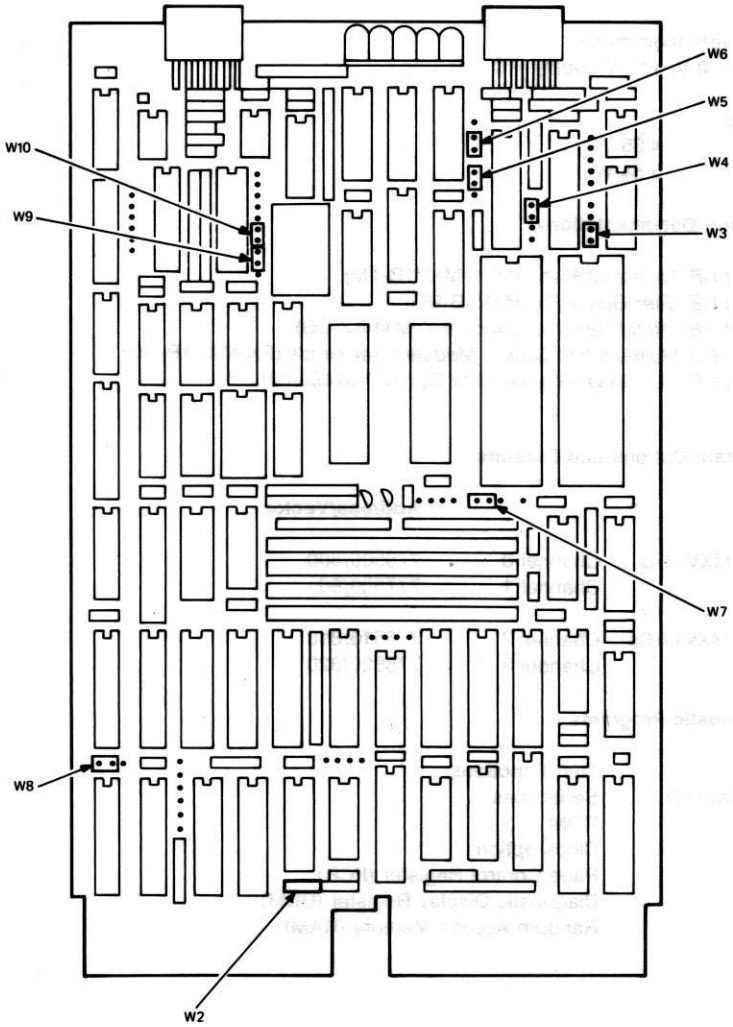
		Address/Vector
One MXV11-B	Channel 0	776500/300
	Channel 1	777560/60
Two MXV11-Bs	Channel 2	776510/310
	Channel 3	776520/320

Diagnostic Programs

	Test Functions
CVMX.BAO	Serial lines
	ROM
	Clock option
	Page Control Register (PCR)
	Diagnostic Display Register (DDM)
	Random Access Memory (RAM)

Default Jumpers

The default jumpers are as shown below.



Default Configuration of Push-On Connectors

Interface Connector Pins

Two 10-pin connectors, one for each serial line, are provided on the MXV11-B module. The connector pins and signal functions are described below.

MXV11-B I/O Connector Pin Functions

Pin	Signal	Function
1	BRCLK	Baud rate clock. This output provides a clock signal at a frequency of 16 times the selected baud rate. This pin is used as an output from the MXV11-B and does not accept external clock inputs.
2	Ground	
3	XMIT+	Transmitter output
4	Ground	
5	Ground	
6	NC	Key, pin not provided
7	RCV–	Receiver input most negative
8	RCV+	Receiver input most positive
9	Ground	
10	+12 V	Power for the DLV11-KA option

Jumpers are used to configure:

Console mode	Reboot
MXV11-B2 boot ROM set	Line time clock
System size	EVENT line
Boot and diagnostic ROMs	Software programmed baud rates
Clock	Battery
Halt	User-supplied ROMs

Baud Rates

Each serial line can be software programmed or strapped to 300, 1200, 9600, or 38,400 baud and is compatible with EIA RS-423 or RS-232 signal levels.

When bit 06 is set, the BEVENT line clamp is removed and LTC is functional. The LTC address is 777546.

CAUTION

There should be only one source drive on the BEVENT line in any system. On most systems, the system power supply provides the bevent signal. this source must be disabled if the mxv11-b is used to drive the line clock.

This register is a write-only register, but generates a reply on DATIO and DATIO B lines. The DDR resides in location 777524 on the I/O page and is enabled when the MXV11-B has its boot and console functions enabled.

Serial Line Unit Baud Rates

			SLU0 (See Note)	
		J0B to GND (J10 to J9)	J0A to GND (J11 to J9)	Baud Rates
J11	J0B	R	R	300*
J10	J0B	R	I	1200
J9	GND	I	R	9600
		I	I	38.4K

			SLU1 (See Note)	
		J1A to GND (J8 to J9)	J1B to GND J7 to J9)	Baud Rates
J9	GND	R	R	9600*
J8	J1A	R	I	38.4K
J7	J1B	I	R	300
		I	I	1200

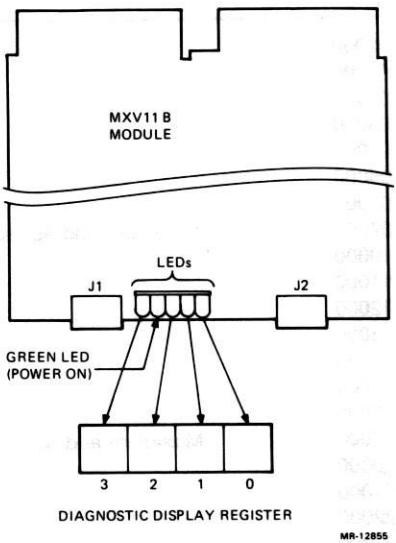
R = jumper removed
I = jumper inserted to ground
*Shipped configuration

NOTE

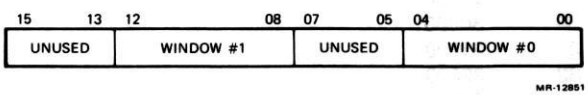
SOFT EN to GND jumper (J14 to J13) must be removed; otherwise these jumpers have no effect. If the SOFT EN to GND jumper (J14 to J13) is installed and PBRE bit 1 is set, baud rates are software controlled.

LED Diagnostic Display Register

The MXV11 has a diagnostic display register (DDR) which has four red LEDs to show system diagnostics and one green LED to indicate power-on.



MXV11-B Diagnostic Register (LEDs)



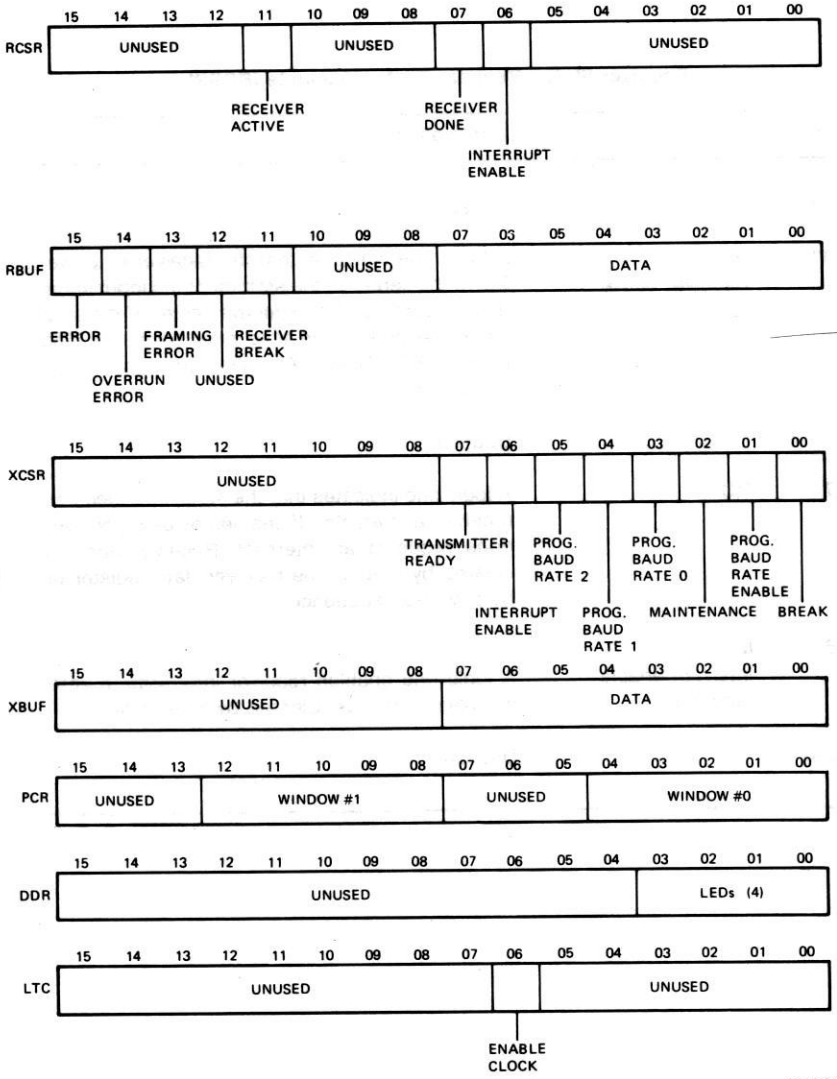
Page Control Register

ROM Window Addresses for 16-, 18-, and 22-bit Q-Bus

Q-Bus	Window 1 Start Addr (octal)	End Addr (octal)	Window 0 Start Addr (octal)	End Addr (octal)
16-bit	165000	165777	173000	173377
18-bit	765000	765777	773000	773377
22-bit	17765000	17765777	17773000	17773377

ROM Window Map

Window Field	Normalized 0 ROM Address	
0	00000	
1	01000	
2	02000	
3	03000	
4	04000	
5	05000	
6	06000	
7	07000	Maximum address for 2K by 8 PROM
10	10000	
11	11000	
12	12000	
13	13000	
14	14000	
15	15000	
16	16000	
17	17000	Maximum address for 4K by 8 PROM
20	20000	
21	21000	
22	22000	
23	23000	
24	24000	
25	25000	
26	26000	
27	27000	
30	30000	
31	31000	
32	32000	
33	33000	
34	34000	
35	35000	
36	36000	
37	37000	Maximum address for 8K by 8 PROM



MXV11-B Register Bit Formats

Receiver Status Register Bit Assignments (RCSR)

Bit		Description
15–12		Unused
11	RA Receiver active read only	A logic one indicates that the receiver is active. Set at the center of the start bit of the input serial data. Cleared at the expected center of the stop bit at the end of the time prior to the leading edge of RCV DONE. Also cleared by power up sequence.
10–8		Unused
7	RD	A logic one indicates that the serial interface has received a character. If enabled by bit 6, receiver done requests an interrupt. Receiver done is cleared by reading the receiver data register or by power-up sequence.
6	IE Interrupt enable read/write	A logic one enables receiver interrupts; a zero disables interrupts. Cleared by initialization.
5–0		Unused

Receiver Data Buffer Bit Assignments (RBUF)

Bit		Description
15	ER Error read only	A logic one indicates that bit 13 and/or bit 14 is a one. Cleared when the bit is read or cleared by power-up sequence.
14	OE Overrun error read only	A logic one indicates a word in the receiver buffer had not been read when another word was received and placed in the receiver buffer. Cleared when read or by power-up sequence.
13	FE Framing error read only	A logic one indicates that a start bit was detected, but there was no corresponding stop bit. A framing error is generated when a break is received. Cleared when read or by power-up sequence.
12		Unused
11	RB Receiver break read only	This bit is set when serial-in (SI) signal goes from a mark to a space and stays in the space condition for 11 bit times after serial reception starts. This bit is cleared when the SI signal returns to the mark condition, or by power-up sequence.
10–8		Unused
7-0	DATA read only	These eight bits hold the most recent byte received. When a new byte is transferred to the data buffer, the RCV DONE in the RCSR is set. Bit 0 is the LSB and bit 7 is the MSB. Cleared by power-up sequence.

Transmitter Status Register Bit Assignments (XCSR)

Bit		Description
15–8		Unused
7	TR Transmitter read read only	A logic one indicates the serial interface is ready to accept a character into the transmitter data register. If enabled by bit 6, transmitter ready requests an interrupt. Transmitter ready is cleared when data is written into the transmitter data register. It is set by power-up sequence.
6	IE Interrupt enable read/write	A logic one enables transmitter interrupts. A logic zero disables interrupts. Cleared by initialization.
5–3	BR2-BR0* Programmable baud rate select read/write	When PBR-bit 1 in XCSR is set, these baud bits determine the baud rate (set by software if SOFT jumper connected to GND). If SOFT jumper is connected to OPEN, baud rate is obtained via wire-wrap. Bits BR2-BR0 are cleared by PBR inhibit (SOFT EN) or by power-up sequence.
2	MAINT Maintenance read/write	This bit facilitates a maintenance self-test. When the bit is set, the the transmitter serial output is connected to the receiver serial input and the external serial input is disconnected. This bit is cleared by initialization.

* Read only as a zero when programmable baud rate inhibit (PBRI) is asserted low. PBRI is asserted low by connecting the SOFT EN to OPEN jumpers (J14 to J15). In this case, the baud rate is determined by the wire-wrap jumpers (J7–J11). Otherwise, with SOFT EN to GND (J14–J13), the bit is read/write. This bit is cleared by power-up sequence or PBRI (SOFT EN to OPEN jumper – J14–J15).

Transmitter Status Register Bit Assigments (XCSR) (Cont)

Bit		Description
1	PBR* Programmable baud rate enable Read/write when software programmable baud rates enabled (SOFT to GND jumper); else read only as 0.	This bit selects between internal and external baud rate selection. When set (enable), the baud rate is determined by the PBR2–0 bits in this register. When clear (inhibit), the baud rate is determined by the J1, J0 wire-wrap pins. This bit is cleared by power-up sequence or SOFT to OPEN jumper connected (programmable baud rate inhibit (J14 to J15).
0	BK Break read/write	When this bit is set, it causes the serial output signal to go to a space condition. A space condition longer than a character time causes a framing error when it is received and is regarded as a break. Cleared by bus initialization.

* Read only as a zero when programmable baud rate inhibit (PBRI) is asserted low. PBRI is asserted low by connecting the SOFT EN to OPEN jumpers (J14 to J15). In this case, the baud rate is determined by the wire-wrap jumpers (J7–J11). Otherwise, with SOFT EN to GND (J14–J13), the bit is read/write. This bit is cleared by power-up sequence or PBRI (SOFT EN to OPEN jumper – J14–J15).

Transmitter Data Buffer Bit Assignments (XBUF)

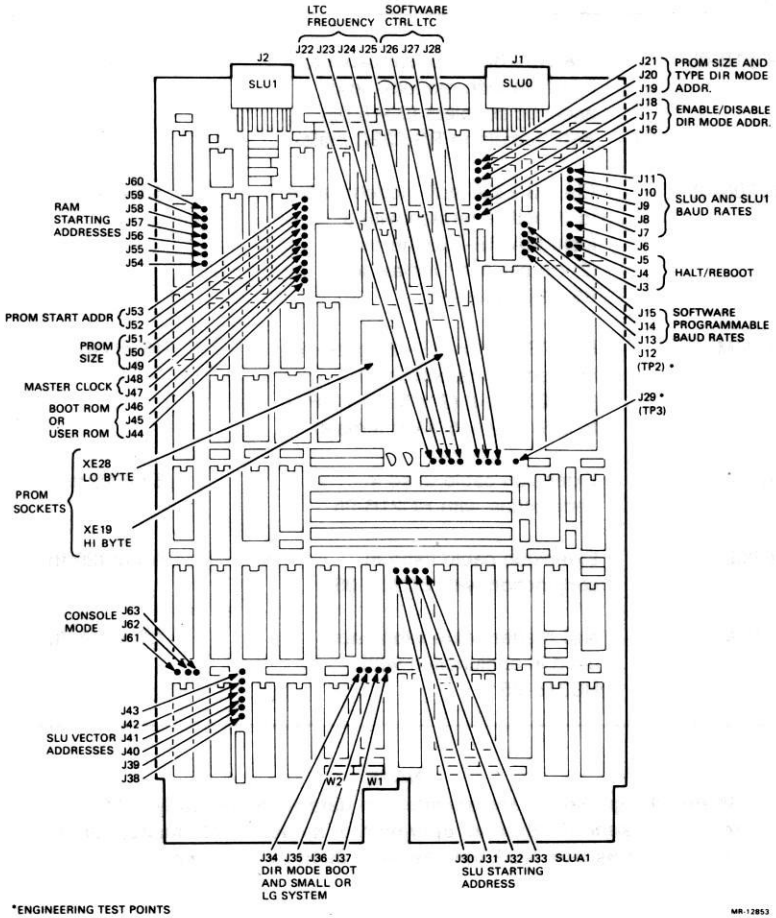
Bit		Description
15–8		Unused
7-0	XMIT DATA BUFFER read/write	Transmitter data buffer – this byte register holds a copy of the most recent byte written into it. When a byte is written into this register, the transmit ready (TR) bit in the XCSR register is cleared. This byte is copied into the transmitter serial output register whenever that register is empty and the bit is clear. The TR bit is set when a byte is copied from the transmitter data buffer into the serial output register. Reading the contents of this register causes no other effect. Cleared by power-up sequence.

Definition of Cables

Cable	Application	Length
BC21B-05	EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5 pin AMP female to RS-232C male)	1.5 m (5 ft)
BC20N-05	EIA RS-232C null modem cable to directly interface with a local EIA RS-232C terminal (2 × 5 pin AMP female to RS-232C female)	1.5 m (5 ft)
BC20M-50	EIA RS-422 or RS-423 cable for high-speed transmission (19,200 baud) (2 × 5 pin AMP female to 2 × 5 AMP female)	15 m (50 ft)
BC05D-10	Extension cable used in conjunction with BC21B-05	3 m (10 ft)
BC05D-25	Extension cable used in conjunction with BC21B-05	7.6 m (25 ft)
BC03M-25	Null modem extension cable used in conjunction with BC21B-05	7.6 m (25 ft)

NOTE

Strapped logic levels are provided on data terminal ready (DTR) and request to send (RTS) to all operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).



MXV11-B Jumper Locations

Jumper Connections for MXV11-B Summary

Jumper	Name	Function	Connection*
J1	Connector for SLU0		
J2	Connector for SLU1	SLU connectors	
J3	HALT		
J4	GND	Halt and reboot functions	POC (W3)
J5	RBOOT		
J6	OPEN		
J7	J1B		
J8	J1A	Serial line unit baud rates	WW
J9	GND		
J10	J0B		
J11	J0A		
J12	TP2	For engineering use	
J13	GND		
J14	SOFT EN	Software programmable	POC (W4)
J15	OPEN	baud rates	
J16	GND		
J17	PG L/DIR H	Enables or disables direct	POC (W5)
J18	OPEN	mode addressing	
J19	AL12H		
J20	NA12H	PROM size and type in	POC (W6)
J21	+5 V	direct mode addressing	
J22	LTC COMM		
J23	50 Hz	Line time clock frequency	WW
J24	60 Hz		
J25	800 Hz		
J26	OPEN		
J27	LTC EN IN	Software control of line	POC (W7)
J28	LTC EN OUT	time clock	
J29	TP3	For engineering use	
J30	SLUA3		
J31	GND	Serial line unit starting	WW
J32	SLUA2	address	
J33	SLUA1		

Jumper Connections for MXV11-B Summary (Cont)

Jumper	Name	Function	Connection*
J34	DIR MODE BOOT		
J35	OPEN	Direct mode boot and	WW
J36	GND	small or large system	
J37	SM/LG		
J38	JU1		
J39	JU2		
J40	GND	Serial line unit vector	WW
J41	JL1	address	
J42	JL2		
J43	JL3		
J44	BOOT L/PROM H		
J45	GND	Boot ROM or user ROM	POC (W9)
J46	OPEN		
J47	CLOCK IN		
J48	CLOCK OUT	Master clock	POC (W10)
J49	PROM 1		
J50	PROM 2		
J51	GND	PROM size and PROM	WW
J52	BSK1	start address	
J53	BSK2		
J54	AJ13		
J55	AJ14		
J56	AJ15	RAM starting address	WW
J57	GND		
J58	AJ16		
J59	AJ17		
J60	AJ18		
J61	OPEN		
J62	GND	Console mode	POC (W8)
J63	CONSOLE		

*POC = Push-on connector
WW = Wire-wrap

NOTE

W1 and W2 are 0 ohm resistors associated with battery backup option. Either one may be inserted but not both. The module is shipped with W2 inserted.

Miscellaneous Jumper Configurations

Connector		Connection	Description
J63 J62 J61	CONSOLE GND OPEN	GND to OPEN (J62 to J61)	Enables console mode. SLU is fixed at address 77560 and vector address at 60. Select SLU 0 address from Table B and vector from Table C.
J63 J62 J61	CONSOLE GND OPEN	CONSOLE to GND (J63 to J62)	Disables console mode. For SLU addresses, refer to Table B and vectors from Table C.
J46 J45 J44	OPEN GND BOOT L/PROM H	BOOT L/PROM H to GND (J44 to J45)	Inserted when MXV11-B2 boot ROM set is installed in sockets XE19 and XE29. Enables the following registers to be addressed if the console GND to OPEN jumper (J62 to J61) is installed: Page control register Line time clock control Diagnostic display register.
J46 J45 J44	OPEN GND BOOT L/PROM H	GND to OPEN (J45 to J46)	Inserted when ROMs are for user code (not bootstrap code). See Table A for addresses.
J37 J36 J35	SM/LG SYS GND OPEN	SM/LG SYS to GND (J37 to J36)	This is installed when the MXV11-B is connected in a Q22 bus backplane. Recognizes BDAL <21:00> L. This jumper must be installed if RAM is addressed above 128K words.
J37 J36 J35	SM/LG SYS GND OPEN	GND to OPEN (J36 to J35)	Installed when the MXV11-B is connected to a 16- or 18-bit Q-BUS. Recognizes BDAL <17:00> L only.
J36 J35 J34	GND OPEN DIRECT MODE BOOT	DIR MODE BOOT to OPEN (J34 to J35)	Module not wired for direct mode boot.

Miscellaneous Jumper Configurations (Cont)

Connector		Connection	Description
J36 J35 J34	GND OPEN DIRECT MODE BOOT	DIR MODE BOOT to GND (J34 to J36)	Module enabled for direct mode boot. This jumper must be installed when the user boot is directly addressed.
J18 J17 J16	OPEN PG L/DIR H GND	PG L/DIR H to GND (J17 to J16)	Enables ROM boot map option and page mode on the MXV11-B. Disables user PROM addresses below 16K.
J18 J17 J16	OPEN PG L/DIR H GND	PG L/DIR H to OPEN (J17 to J18)	Enables PROM sockets XE19 and XE28 to be used for user defined PROMs. In this case, these sockets can only be addressed in memory locations below the 16K word boundary.
J48 J47	CLOCK OUT CLOCK IN	CLOCK OUT to CLOCK IN (J48 to J47)	Factory test. Do not remove. This is the master clock, and provides on-board refresh and the charge pump to generate −12 V.
J3 J4 J5 J6	HALT GND RBOOT OPEN	HALT to GND (J3 to J4)	Enables SLU 1 (console port) to halt the processor upon receiving a break character.
J3 J4 J5 J6	HALT GND RBOOT OPEN	HALT not connected to GND	Disables CPU halt function.
J3 J4 J5 J6	HALT GND RBOOT OPEN	RBOOT to GND	Causes a system reboot when a break condition is received from SLU 1. Forces BDC OK-H low on the bus.

NOTE

HALT to GND (J3 to J4) and RBOOT to GND (J5 to J4) cannot be simultaneously jumpered.

Miscellaneous Jumper Configurations (Cont)

Connector		Connection	Description
J3 J4 J5 J6	HALT GND RBOOT OPEN	GND to OPEN (J4 to J3)	Disables reboot function.
J26 J27 J28	OPEN LTC EN IN LTC EN OUT	LTC EN IN to LTC EN OUT (J27 to J28)	Allows LTC to be software controlled. Enables control of BEVENT L on the bus via bit 06 of the LTC register. When bit 6 of LTC register is 0, BEVENT L will be asserted constantly low. This inhibits LTC interrupts. To address the LTC register (777546), the MXV11-B must be in boot mode (BOOT L/PROM H to GND) (J44 to J45) and SLU1 must be the console port (CONSOLE to GRD removed).
J26 J27 J28	OPEN LTC EN IN LTC EN OUT	LTC EN IN to OPEN (J27 to J26)	Prevents bits 06 of the LTC register from controlling the BEVENT L line.
J22 J23	LTC COMM 50 Hz	LTC COMM to 50 Hz (J22 to J23)	When installed, the BEVENT line is driven from a 50 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line.
J24	60 Hz	LTC COMM to 60 Hz (J22 to J24)	When installed, the BEVENT line is driven from a 60 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line.

CAUTION

LTC EN IN to LTC EN OUT (J27 to J28) should not be connected if the CPU has an LTC control register.

Miscellaneous Jumper Configurations (Cont)

Connector		Connection	Description
J25	800 Hz	LTC COMM to 800 Hz (J22 to J25)	When installed, the BEVENT line is driven from an 800 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line.
J15 J14 J13	OPEN SOFT EN GND	SOFT EN to GND (J14 to J13)	Enables software programmable baud rates for both SLU1 and SLU0 via the CSR. The baud rate jumpers in Table B have no effect if the PBRE bit is set.
J15 J14 J13	OPEN SOFT EN GND	SOFT EN to OPEN (J14 to J15)	Baud rates are selected from Table B.
W1		W1 (0 ohm resistor) connected	Battery backup. +5 V is supplied by user on backplane pin AV1. DIGITAL does not supply battery backup.
W2		W2 (0 ohm resistor) connected	No battery backup.
J21 J20 J19	+5 V NA12H BA12H	NA12H to +5 V (Normalized address 12) (J20 to J21) to (Buffered Address line 12)	Specifies 2K user UVROMs (2716) installed and direct mode addressing
J21 J20 J19	+5 V NA12H BA12H	NA12H to BA12H (J20 to J19)	Specifies 4K or 8K user-supplied ROM in direct mode addressing.

NOTE

One of these jumpers (50, 60, or 800 Hz) should be installed: 1) If no external BEVENT source is provided in the system, and 2) If the user desires this source. Power supplies manufactured by DIGITAL normally supply BEVENT L to the backplane.

NOTE

There are cases where none of these jumpers (+5 V, NA4H, and AL12H) should be connected. In these cases, the push-on connector must be completely removed or must be connected to one of the outside pins to hold the connector. There is no open pin associated with these jumpers. For example, if 2K non-UV PROMs or the MXV11-B2 ROM is to be installed, these jumpers are all disconnected.

Table A. Jumpers for PROM Starting Address

		BSK2 to GND (J53 to J51)	BSK1 to GND (J52 to J51)	User PROM Starting Address (octal) (Note)
J51	GND	R	R	000000*
J52	BSK1	R	I	020000
J53	BSK2	I	R	040000
	I	I	060000	

R = jumper removed
I = jumper inserted to ground
* Shipped configuration. Remove all jumpers from BSK1 (J52) and BSK2 (J53) if not in user mode.

NOTE

These addresses are for user supplied ROMs only. Jumpers BOOT L/PROM H to GND (J44 to J45) and PG L/DIR H to GND (J17 to J16) must be removed.

Table B. Serial Line Unit Starting Address Jumpers

		SLUA3 to GND (J30 to J31)	SLUA2 to GND (J32 to J31)	SLU1 to GND (J33 to J31)	Starting Address SLU0	SLU1 (See Note)
J33	SLUA1	R	R	R	776500*	776510*
J32	SLUA2	R	R	I	776510	776520
J31	GND	R	I	R	776520	776530
J30	SLUA3	R	I	I	776530	776540
		I	R	R	776540	776550
		I	R	I	776550	776560
		I	I	R	776560	776570
		I	I	I	776570	776600

R = jumper removed
I = jumper inserted to ground
*Shipped configuration

NOTE

If the GND to OPEN jumper (J62 to J61) is installed (console enabled), the SLU1 address is fixed at the standard console address of 777560 and this column does not apply.

Table C. Jumpers for SLU Vector Addresses

		JU2 to GND (J39 to J40)	JU1 to GND (J38 to J40)	JL3 to GND (J43 to J40)	JL2 to GND (J42 to J40)	JL1 to GND (J41 to J40)	SLU0	SLU1 (See Note)
J43	JL3	R	R	R	R	R	300*	310*
J42	JL2	R	R	R	R	I	010	020
J41	JL1	R	R	R	I	R	020	030
J40	GND	R	R	R	I	I	030	040
J39	JU2	R	R	I	R	R	040	050
J38	JU1	R	R	I	R	I	050	060
		R	R	I	I	R	060	070
		R	R	I	I	I	070	100
		R	I	R	R	R	100	110
		R	I	R	R	I	110	120
		R	I	R	I	R	120	130
		R	I	R	I	I	130	140
		R	I	I	R	R	140	150
		R	I	I	R	I	150	160
		R	I	I	I	R	160	170
		R	I	I	I	I	170	200
		I	R	R	R	R	200	210
		I	R	R	R	I	210	220
		I	R	R	I	R	220	230
		I	R	R	I	I	230	240
		I	R	I	R	R	240	250
		I	R	I	R	I	250	260
		I	R	I	I	R	260	270
		I	R	I	I	I	270	300
		I	I	R	R	R	300	310
		I	I	R	R	I	310	320
		I	I	R	I	R	320	330
		I	I	R	I	I	330	340
		I	I	I	R	R	340	350
		I	I	I	R	I	350	360
		I	I	I	I	R	360	370
		I	I	I	I	I	370	Undefined

I = jumper inserted from specified pin to ground. Where multiple connections are made, they are daisy-chained.
R = jumper removed
*Shipped configuration

NOTE

If the GND to OPEN jumper (J62 to J61) is installed (console enabled), SLU1 vector address is fixed at 60 and this column does not apply.

PROM Jumpers

		NA12H to BA12H (J20 to J19)	NA12H to +5 V (J20 to J21)	Description
J19	BA12H	R	R	
J20	NA12H	I	R	
J21	+5 V	R	I	Page mode – Boot ROM for 2K by 8 non-UV PROMs, 4K by 8 or 8K by 8 PROMs Direct mode – for 2K by 8, non-UV PROMs, 4k by 8, or 8K by 8 PROMs* Direct mode – for 2K by 8 UV PROMs

R = jumper removed
I = jumper inserted
*Shipped configuration

Jumpers to Configure PROM Size

		PROM 2 to GND (J50 to J51)	PROM 1 to GND (J49 to J51)	PROM Size	
J51	GND	R	R	No ROMs*	
J50	PROM 2	R	I	2K by 8	
J49	PROM 1	I	R	4K by 8	
			I	I	8K by 8†

R = jumper removed
I = jumper inserted

* Shipped configuration. Additional jumpers are required depending on user mode/boot mode and direct addressing page addressing. Refer to the last three tables in this section.

† If the MXV11-B2 Boot Diagnostic ROM set is installed, install PROM 2 to PROM 1 to GND jumper (J50 to J49 to J51).

RAM Starting Address Jumpers

			AJ18 to GND (J60 to J57)	AJ17 to GND (J59 to J57)	AJ16 to GND (J58 to J57)	AJ15 to GND (J56 to J57)	AJ14 to GND (J55 to J57)	AJ13 to GND (J54 to J57)	RAM Starting Address (Words)
J60	AJ18	00	R	R	R	R	R	R	0*
J59	AJ17	01	R	R	R	R	R	I	4K
J58	AJ16	02	R	R	R	R	I	R	8K
J57	GND	03	R	R	R	R	I	I	12K
J56	AJ15	04	R	R	R	I	R	R	16K
J55	AJ14	05	R	R	R	I	R	I	20K
J54	AJ13	06	R	R	R	I	I	R	24K
		07	R	R	R	I	I	I	28K
		10	R	R	I	R	R	R	32K
		11	R	R	I	R	R	I	36K
		12	R	R	I	R	I	R	40K
		13	R	R	I	R	I	I	44K
		14	R	R	I	I	R	R	48K
		15	R	R	I	I	R	I	52K
		16	R	R	I	I	I	R	56K
		17	R	R	I	I	I	I	60K
		20	R	I	R	R	R	R	64K
		21	R	I	R	R	R	I	68K†
		22	R	I	R	R	I	R	72K†
		23	R	I	R	R	I	I	76K†
		24	R	I	R	I	R	R	80K†
		25	R	I	R	I	R	I	84K†
		26	R	I	R	I	I	R	88K†
		27	R	I	R	I	I	I	92K†
		30	R	I	I	R	R	R	96K†
		31	R	I	I	R	R	I	100K†
		32	R	I	I	R	I	R	104K†
		33	R	I	I	R	I	I	108K†
		34	R	I	I	I	R	R	112K†
		35	R	I	I	I	R	I	116K†
		36	R	I	I	I	I	R	120K†
		37	R	I	I	I	I	I	124K†
		40	I	R	R	R	R	R	128K†
		41	I	R	R	R	R	I	132K†
		42	I	R	R	R	I	R	136K†
		43	I	R	R	R	I	I	140K†
		44	I	R	R	I	R	R	144K†
		45	I	R	R	I	R	I	148K†
		46	I	R	R	I	I	R	152K†
		47	I	R	R	I	I	I	156K†

RAM Starting Address Jumpers (Cont)

	AJ18 to GND (J60 to J57)	AJ17 to GND (J59 to J57)	AJ16 to GND (J58 to J57)	AJ15 to GND (J56 to J57)	AJ14 to GND (J55 to J57)	AJ13 to GND (J54 to J57)	RAM Starting Address (Words)
50	I	R	I	R	R	R	160K†
51	I	R	I	R	R	I	164K†
52	I	R	I	R	I	R	168K†
53	I	R	I	R	I	I	172K†
54	I	R	I	I	R	R	176K†
55	I	R	I	I	R	I	180K†
56	I	R	I	I	I	R	184K†
57	I	R	I	I	I	I	188K†
60	I	I	R	R	R	R	192K†
61	I	I	R	R	R	I	196K†
62	I	I	R	R	I	R	200K†
63	I	I	R	R	I	I	204K†
64	I	I	R	I	R	R	208K†
65	I	I	R	I	R	I	212K†
66	I	I	R	I	I	R	216K†
67	I	I	R	I	I	I	220K†
70	I	I	I	R	R	R	224K†
71	I	I	I	R	R	I	228K†
72	I	I	I	R	I	R	232K†
73	I	I	I	R	I	I	236K†
74	I	I	I	I	R	R	240K†
75	I	I	I	I	R	I	244K†
76	I	I	I	I	I	R	248K†
77	I	I	I	I	I	I	252K†

I = jumper inserted from designated pin to GND. Where multiple connections are made, they are daisy-chained.

R = jumper removed.

* Shipped configuration

† To use address above 64K words, SM/LG SYS TO GND jumper (J37 to J36) must be installed

NOTE

Be careful when configuring the MXV11-B RAM when ROM is used in the USER ROM address space. USER ROM address space is defined as bus addresses 0–16K, (00000–100000) on 4K boundaries. The RAM start address must be higher than the last location of the ROM or dual responses from both the RAM and ROM will occur. The chart below shows several examples of right and wrong ways of assigning RAM memory start addresses.

ROM Size	ROM Start	RAM Start	RAM End	Comments
8K	0K	4K	68K	Wrong, 4K overlap (4K→8K)
8K	4K	0K	64K	Wrong, 8K overlap (4K→12K)
4K	0K	4K	68K	Right, no overlap
4K	0K	12K	76K	Right, no overlap‡
8K	4K	12K	76K	Right

‡ Address space gap usually not recommended but up to user to decide depending on application.

Jumper Connections for PROM Sizes in User Mode

Jumpers		No PROMs	2K by 8	4K by 8	8K by 8
J16	(GND)	J17 to J18	J17 to J18	J17 to J18	J17 to J18
J17	(PG L/DIR H)				
J18	(OPEN)				
J19	(BA12H)	J19 to J20	J20 to J21	J19 to J20	J19 to J20
J20	(NA12H)				
J21	(+5 V)				
J44	(BOOT L/PROM H)	J45 to J46	J45 to J46	J45 to J46	J45 to J46
J45	(GND)				
J46	(OPEN)				
J49	(PROM1)	–	J49 to J51	J50 to J51	J49 to J50 to J51
J50	(PROM2)				
J51	(GND)				

NOTE

Jumper connections are indicated. For example, in the 2K by 8 PROM, J17 is connected to J18, J20 is connected to J21, J45 is connected to J46, and J49 is connected to J51.

Jumper Connections for PROM Sizes in Boot Mode (Page Addressing)

Jumpers	No PROMs	2K by 8*	4K by 8	8K by 8
J16 (GND) J17 (PG L/DIR H) J18 (OPEN)	J17 to J18	J16 to J17	J16 to J17	J16 to J17
J19 (BA12H) J20 (NA12H) J21 (+5 V)	J19 to J20	–	J19 to J20	J19 to J20
J44 (BOOT L/PROM H) J45 (GND) J46 (OPEN)	J45 to J46	J44 to J45	J44 to J45	J44 to J45
J49 (PROM1) J50 (PROM2) J51 (GND)	–	J49 to J51	J50 to J51	J49 to J50 to J51

*2K by 8 UV PROM cannot be used in page mode.

NOTE

Jumper connections are indicated. For example, in the 8K by 8 PROM, J16 is connected to J17, J19 is connected to J20, J44 is connected to J45 and J49, J50 and J51 are connected.